PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Lindholm et al.

Application No.: 09/960,004

Filed: September 20, 2001

For: MASKING SYSTEM AND METHOD FOR A GRAPHICS PROCESSING FRAMEWORK EMBODIED ON A SINGLE SEMICONDUCTOR PLATFORM

Attorney Docket No.: NVIDP008B/P000057

Examiner: Unassigned

Group Art Unit: 2671

Date: June 28, 2002

COPY

CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being deposited with the US Patent & Trademark Office via facsimile to fax number (703) 872-9314 on June 28, 2002.

Signed: Erica L. Mann
Erica L. Mann

Commissioner for Patents
Box Fee Amendment
Washington, DC 20231

Sir:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated as shown below.

	Claims Remaining After Amendment		Highest Previously Paid For Extra	Present	SMALL ENTITY RATE FEE		OR	LARGE ENTITY RATE FEE
TOTAL CLAIMS	55	-	22	33	X09 = $	OR	X18 =	$594
INDEP CLAIMS	09	-	04	05	X42 = $	OR	X84 =	$420
[ ] Multiple Dependent Claim Present and Fee Not Previously Paid					$130			$0
				TOTAL	$			$1,014.00

☐ Applicant(s) hereby petition for a month extension of time to respond to the outstanding Office Action.

☐ Applicant(s) believe that no (additional) Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to Deposit Account No. 50-1351.

☐ Enclosed is our Check No. in the amount of $ to cover the additional claim fee and/or extension of time fees.

☒ If the required fees are missing or any additional fees are required to facilitate filing the enclosed response, please charge such fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP008B). A copy of this sheet is enclosed for billing purposes.

Respectfully submitted,
Silicon Valley IP Group, LLC.

Kevin J. Zilka
Registration No. 41,429

P.O. Box 721120
San Jose, CA 95172-1120
Telephone: (408) 971-2573

(Revised 1/96)

PATENT
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	Docket: NVIDP008B/P000057
Lindholm et al.	Examiner: Vo, C.
Serial No.: 09/960,004	
Filed: September 20, 2001	
For: MASKING SYSTEM AND METHOD FOR A GRAPHICS PROCESSING FRAMEWORK EMBODIED ON A SINGLE SEMICONDUCTOR PLATFORM	Date: June 28, 2002

CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being deposited with the US Patent & Trademark Office via facsimile to fax number (703) 872-9314 on June 28, 2002

Signed: Erica J. Mann
Erica Mann

PRELIMINARY AMENDMENT C

Commissioner for Patents
and Trademarks
Washington, DC 20231

Dear Sir:

Please enter the following preliminary amendments to the pending application.

IN THE CLAIMS

Please add claims 48-80 as follows:

48. (New) A graphics pipeline system with an integrated masking operation, comprising:

a transform module positioned on a single semiconductor platform for transforming graphics data;

a lighting module positioned on the same single semiconductor platform as the transform module, the lighting module being for performing lighting operations on the graphics data;

a set-up module positioned on the same single semiconductor platform as the transform module and the lighting module, the set-up module being for setting up the graphics data; and

a rendering module positioned on the same single semiconductor platform as the transform module, the lighting module, and the set-up module, the rendering module being for rendering the graphics data;

wherein a masking operation is capable of being performed utilizing the single semiconductor platform.

49. (New) The system as recited in claim 48, wherein the masking operation includes a 2-bit write mask for providing control to a word level of a buffer address.

50. (New) The system as recited in claim 48, wherein the masking operation includes individually masking a write operation to at least one register component such that unmasked components are taken from the register and masked components are bypassed.

51. (New) The system as recited in claim 48, wherein the masking operation masks an enabled bit of a control vector for allowing analysis of all remaining bits after execution of the masking operation.

52. (New) The system as recited in claim 51, wherein the masking operation masks vector vertex data for converting the vector vertex data to scalar vertex data.

53. (New) The system as recited in claim 48, wherein the masking operation is associated with an ambient attribute.

54. (New) The system as recited in claim 48, wherein the masking operation is associated with a diffuse attribute.

55. (New) The system as recited in claim 48, wherein the masking operation is associated with a specular attribute.

56. (New) The system as recited in claim 48, wherein the single semiconductor platform is adapted for coupling to a central processing unit for receiving instructions therefrom.

57. (New) A method for graphics processing, comprising:
transforming graphics data from a first space to a second space;
lighting the graphics data;
performing a masking operation on the graphics data;
setting up the graphics data; and
rendering the graphics data;
wherein the graphics data is set up, transformed and lighted, and the masking operation is performed, on a single semiconductor platform.

58. (New) The method as recited in claim 57, wherein the masking operation includes a 2-bit write mask for providing control to a word level of a buffer address.

59. (New) The method as recited in claim 57, wherein the masking operation includes individually masking a write operation to at least one register component such that unmasked components are taken from the register and masked components are bypassed.

60. (New) The method as recited in claim 57, wherein the masking operation masks an enabled bit of a control vector for allowing analysis of all remaining bits after execution of the masking operation.

61. (New) The method as recited in claim 60, wherein the masking operation masks vector vertex data for converting the vector vertex data to scalar vertex data.

62. (New) The method as recited in claim 57, wherein the masking operation is associated with an ambient attribute.

63. (New) The method as recited in claim 57, wherein the masking operation is associated with a diffuse attribute.

64. (New) The method as recited in claim 57, wherein the masking operation is associated with a specular attribute.

65. (New) A single-platform graphics pipeline system with an integrated masking operation, comprising:

a transform module positioned on a single semiconductor platform for transforming graphics data;

a lighting module positioned on the same single semiconductor platform as the transform module, the lighting module being for performing lighting operations on the graphics data;

a set-up module positioned on the same single semiconductor platform as the transform module and the lighting module, the set-up module being for setting up the graphics data; and

a rendering module positioned on the same single semiconductor platform as the transform module, the lighting module, and the set-up module, the rendering module being for 3-D rendering of the graphics data;

wherein the single semiconductor platform is adapted for coupling to a central processing unit for receiving instructions therefrom;

wherein a masking operation is capable of being performed utilizing the single semiconductor platform;

wherein the single semiconductor platform is capable of operating with an application program interface.

66. (New) The system as recited in claim 65, wherein the masking operation includes a 2-bit write mask for providing control to a word level of a buffer address.

67. (New) The system as recited in claim 65, wherein the masking operation includes individually masking a write operation to at least one register component such that unmasked components are taken from the register and masked components are bypassed.

68. (New) The system as recited in claim 65, wherein the masking operation masks an enabled bit of a control vector for allowing analysis of all remaining bits after execution of the masking operation.

69. (New) The system as recited in claim 65, wherein the masking operation is associated with an ambient attribute.

70. (New) The system as recited in claim 65, wherein the masking operation is associated with a diffuse attribute.

71. (New) The system as recited in claim 65, wherein the masking operation is associated with a specular attribute.

72. (New) A method for graphics processing, comprising:
transforming graphics data from a first space to a second space;
lighting the graphics data;
performing a masking operation on the graphics data;
setting up the graphics data; and
3-D rendering the graphics data;
wherein the graphics data is set up, transformed and lighted, and the masking operation is performed, on a single semiconductor platform;
wherein the single semiconductor platform also operates with an application program interface.

73. (New) The method as recited in claim 72, wherein the masking operation includes a 2-bit write mask for providing control to a word level of a buffer address.

74. (New) The method as recited in claim 72, wherein the masking operation includes individually masking a write operation to at least one register component such that unmasked components are taken from the register and masked components are bypassed.

75. (New) The method as recited in claim 72, wherein the masking operation masks an enabled bit of a control vector for allowing analysis of all remaining bits after execution of the masking operation.

76. (New) The method as recited in claim 72, wherein the masking operation is associated with an ambient attribute.

77. (New) The method as recited in claim 72, wherein the masking operation is associated with a diffuse attribute.

78. (New) The method as recited in claim 72, wherein the masking operation is associated with a specular attribute.

79. (New) The method as recited in claim 72, wherein the single semiconductor platform is adapted for coupling to a central processing unit for receiving instructions therefrom.

80. (New) A single-platform graphics pipeline system with an integrated masking operation, comprising:

a transform module positioned on a single semiconductor platform for transforming graphics data;

a lighting module positioned on the same single semiconductor platform as the transform module, the lighting module being for performing lighting operations on the graphics data;

a set-up module positioned on the same single semiconductor platform as the transform module and the lighting module, the set-up module being for setting up the graphics data;

a rendering module positioned on the same single semiconductor platform as the transform module, the lighting module, and the set-up module, the rendering module being for 3-D rendering of the graphics data; and

memory positioned on the same single semiconductor platform as the transform module, the lighting module, the set-up module, and the render module for storing the graphics data;

wherein the single semiconductor platform is adapted for coupling to a central processing unit for receiving instructions therefrom;

wherein a masking operation is performed utilizing the single semiconductor platform;

wherein a scissor operation is performed utilizing the single semiconductor platform;

wherein a clipping operation is performed utilizing the single semiconductor platform;

wherein the graphics data is blended utilizing the single semiconductor platform for blending triangles represented by vertex data associated with the graphics data;

wherein a vertex fog operation is performed on the graphics data utilizing the single semiconductor platform;

wherein the single semiconductor platform operates with a Direct3D application program interface;

wherein the single semiconductor platform also operates with an OpenGL application program interface.

REMARKS

The claims have been amended for clarifying what is claimed in the present application. No new matter has been added.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. If any fees are due in connection with the filing of this paper, then the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP008B/P000057). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
Silicon Valley IP Group, LLC.

Kevin J. Zilka
Registration No. 41,429

P.O. Box 721120
San Jose, CA 95172
Telephone: (408) 505-5100

SILICON VALLEY IP GROUP, LLC.

303 ALMADEN BLVD., #600
SAN JOSE, CA 95110

TELEPHONE (408) 971-2573
FAX (408) 971-4660

FAX COVER SHEET

Date:	June 28, 2002	**Phone Number**	**Fax Number**
To:	Examiner Vo		(703) 872-9314
From:	Kevin J. Zilka		

Docket No.: NVIDP008B/P000057 **Application No.: 09/960,004**

Total Number of Pages Being Transmitted, Including Cover Sheet: 11

Message:

Please enter this amendment into record for application serial number 09/960,004.

Thank you,
Kevin J. Zilka

☐ ***Original to follow Via Regular Mail*** ***X Original will Not be Sent*** ☐ ***Original will follow Via Overnight Courier***

IF YOU DO NOT RECEIVE ALL PAGES OR IF YOU ENCOUNTER
ANY OTHER DIFFICULTY, PLEASE PHONE Erica
AT (408) 971-2573 AT YOUR EARLIEST CONVENIENCE

HP Fax K1220

Log for
SVIPG
408 971 4660
Jun 28 2002 3:23pm

Last Transaction

Date	Time	Type	Identification	Duration	Pages	Result
Jun 28	3:20pm	Fax Sent	917038729314	3:39	11	OK

TO:Auto-reply fax to 4[redacted]71 4660 COMPANY:

Auto-Reply Facsimile Transmission

COPY

UNITED STATES PATENT AND TRADEMARK OFFICE

TO: Fax Sender at 408 971 4660

Fax Information
Date Received: 6/28/02 6:21:31 PM [Eastern Daylight Time]
Total Pages: 11 (including cover page)

ADVISORY: This is an automatically generated return receipt confirmation of the facsimile transmission received by the Office. Please check to make sure that the number of pages listed as received in Total Pages above matches what was intended to be sent. Applicants are advised to retain this receipt in the unlikely event that proof of this facsimile transmission is necessary. Applicants are also advised to use the certificate of facsimile transmission procedures set forth in 37 CFR 1.8(a) and (b), 37 CFR 1.6(f). Trademark Applicants, also see the Trademark Manual of Examining Procedure (TMEP) section 702.04 et seq.

Received Cover Page ========>

Jun 28 02 03:20p SVIPG 408 971 4660 p.1

SILICON VALLEY IP GROUP, LLC.

303 ALMADEN BLVD., #600
SAN JOSE, CA 95110

TELEPHONE (408) 971-2573
FAX (408) 971-4660

FAX COVER SHEET

Date: June 28, 2002	Phone Number	Fax Number
To: Examiner Vo		(703) 872-9314
From: Kevin J. Zilka		

Docket No.: NVIDP008B/P000057 Application No.: 09/960,004

Total Number of Pages Being Transmitted, Including Cover Sheet: 11

Message:

Please enter this amendment into record for application serial number 09/960,004.

Thank you,
Kevin J. Zilka

☐ *Original to follow Via Regular Mail* X *Original will Not be Sent* ☐ *Original will follow Via Overnight Courier*

IF YOU DO NOT RECEIVE ALL PAGES OR IF YOU ENCOUNTER ANY OTHER DIFFICULTY, PLEASE PHONE [redacted] AT (408) 971-2573 AT YOUR EARLIEST CONVENIENCE

Received from <408 971 4660> at 6/28/02 6:21:31 PM [Eastern Daylight Time]